Zero-Voltage and Zero-Current-Switching Dual-Transformer-Based Full-Bridge Converter with Current Doubler Rectifier

Lei Zhao, *Member*, *IEEE*, Jikai Chen, Tongxin Chen, Yi Shi, Zhun Fan and Zhemin Zhuang

***Abstract*—A novel dual-transformer-based full-bridge (DT-FB) converter with current doubler rectifier (CDR), which can solve the drawbacks of existing FB converters, is proposed in this paper. In the primary side of proposed converter, two switching legs, two transformers and two blocking capacitors form two half-bridge inverters, respectively. The secondary side composes of two output filter inductors and four power diodes, which connect with the form of CDR. By employing this structure, a wide range of zero voltage switching for leading-leg and zero current switching for lagging-leg can be achieved. In the proposed converter, the output power is shared by two small-sized transformers and inductors instead of large-sized ones, which contributes to the improvement of power density and efficiency. Compared with the traditional FB converter with CDR, the proposed converter can obtain higher voltage gain, better rectified voltage and lower current ripple. The operation principle, theoretical analysis and design considerations of the proposed converter are described in this paper. A prototype with 300-380 V input and 100 V/ 10 A output is designed and tested to confirm the effectiveness of the proposed converter.**

Index Terms* — *full-bridge converter; zero-voltage and zero-current switching (ZVZCS); current doubler rectifier.

I. Introduction

Phase-shifted full-bridge (PSFB) converter is one of the most attractive topologies for medium and high power applications because of natural zero-voltage switching (ZVS) capability, simple structure and high efficiency [1-5]. In the rectified stage of PSFB converter, full-bridge rectifier (FBR), center-tapped rectifier (CTR) and current doubler rectifier (CDR) can be adopted to suit for various applications. FBR has the lowest voltage stress and transformer voltage-ampere requirement but the highest diode loss, and it is widely applied in high voltage application. On the contrary, CTR has high voltage stress and poor transformer utilization factor but low diode loss, and it suits for the application with low output voltage. As a favorable combination of FBR and CTR, CDR addresses both diode loss and transformer conduction loss, and it is one of effective solutions for the application with high current [6-10].

The traditional PSFB converter has some fundamental disadvantages. First, at light loads, the lagging-leg switches lost the ZVS capability and the conversion efficiency is severely degraded because the available ZVS energy stored in the leakage inductor is insufficient to completely discharge or charge the junction capacitors of switches. Second, the rectifier has large voltage ringing which is caused by the resonance between junction capacitor of diode and leakage inductor. In order to relieve the voltage ringing and to bear the peak value of rectified voltage, snubber circuits and high-voltage rating diodes are needed, resulting in the increase in size, weight and power loss. Another drawback of PSFB converter is the excessive circulating current during the freewheeling interval. The conversion efficiency is significantly affected by the range of input/output voltage [11-13].

Over the past decades, many novel full-bridge (FB) converters have been proposed to solve the aforementioned disadvantages. The ZVS range can be effectively extended by introducing some auxiliary circuits with inductive components. In [14-16], two independent inductors are paralleled with the primary switches and they can be considered as constant current sources during the ZVS transitions. The auxiliary inductors guarantee ZVS under all operating conditions. However, the current stress and conduction loss of switches are increased drastically. In [17,18], a coupled inductor is introduced into the traditional PSFB converters and the peak value of auxiliary current source can be adaptively varied with load current. Therefore, the primary conduction losses caused by the auxiliary current source networks are significantly reduced. The major deficiencies of these converters are too many auxiliary components and high additional core loss. In order to suppress the secondary voltage ringing, the clamp circuits are introduced into the primary side [12,19] or secondary side [20,21] of PSFB converters. The peak value of voltage ringing can be well clamped. However, the problems of narrow ZVS range and primary circulating current are still not solved in these converters. Additionally, some zero-voltage and zero-current switching (ZVZCS) converters are presented to

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remove the primary circulating current [22-25]. In these converters, the leading switches are turned-on with ZVS in the same way as that of the traditional PSFB converter and MOSFETs are employed. The lagging switches are turned-off with zero current by introducing an auxiliary voltage source to reset primary current during freewheeling interval, thus, IGBTs can be employed. Compared to MOSFETs, IGBTs have lower conduction loss due to their fixed collector-emitter voltage drop, which are preferred devices in high power applications. Another advantage of these converters is that the soft-switching conditions are easily satisfied. The main disadvantage is that the primary power cannot be transferred to output side during freewheeling interval, which results in large requirement of output filter and high voltage stress of rectified diodes in variable input voltage applications.

Recently, some dual-transformer-based full-bridge (DT-FB) converters are attractive due to their outstanding performance. In [26-29], the main transformer is replaced by two small-sized transformers and the FB converter is divided into two half-bridge (HB) converters. In [30-34], an auxiliary transformer, blocking capacitors and the lagging-leg switches construct a novel half-bridge converter and it is integrated with the traditional PSFB converter. In these converters, the output power is shared by the two transformers and one of the transformers can continuously transfer the primary energy to the secondary side, which is beneficial for the reduction of circulating current, output filter requirement and secondary voltage stress. Moreover, a wide ZVS range can be achieved since the additional transformer is paralleled with the lagging-leg and the available ZVS energy is enhanced. In the secondary side of these converters, different rectifiers can be adopted to suit for various applications. In [27,30,31], FBR is adopted and the output voltage is larger than 200V. In [26,33,34], CTR is adopted and the output voltage is lower than 100 V. The matched applications for the DT-FB converters with FBR and CTR are the same as that for the traditional PSFB converters with FBR and CTR. Moreover, by combining the structure of FBR and CTR, we proposed a novel DT-FB converter with hybrid rectifier (Hyb-R), and its performance is the best compared with the DT-FB converters with FBR and CTR under the medium voltage condition [28]. The PSFB converter with CDR has been widely adopted for the application with high output current but the corresponding DT-FB converter has never been proposed. Considering the advantages of CDR, such as simple structure, low conduction loss and high power capacity, it is necessary to study how to introduce CDR into the DT-FB converter.

This paper proposes a DT-FB converter with CDR for the first time. The DT-FB converters with three basic rectifiers are found now and the family of DT-FB converters are enriched. Fig.1 shows the circuit configuration of proposed converter. As shown in Fig.1, the FB inverter is divided into two HB inverters in the primary side. Q_1, Q_3, T_1 and C_1 form the leading-HB inverter, and Q_2, Q_4, T_2 and C_2 form the lagging-HB inverter. In the secondary side, the CDR circuit consists of two inductors and four power diodes. The leading-leg switches Q_1-Q_3 can achieve ZVS operation in the same manner as that of the traditional PSFB converter, and they are easy to realize ZVS. The voltage ripple of C_1 can be used as a voltage source to reset the primary current of lagging-HB, which makes it possible to achieve ZCS operation for lagging-leg switches Q_2-Q_4. By using the ZVZCS technique, the primary circulating current is removed and a wide range of soft-switching operation is easily realized. Moreover, the primary power can be continuously transferred to output side through the introduced dual transformers and the current ripple of inductor is significantly reduced, which overcomes the disadvantage of traditional ZVZCS converters. Compared with the existing DT-FB converters, the proposed converter has the advantages of low conduction loss of primary switches, less number of additional components and simple soft-switching conditions.

The operation principle of proposed converter is described in depth in Section II. Section III and Section IV present the main features and design considerations, respectively. In Section V, the theory analysis is verified by an experimental prototype with 300~380 V input voltage and 100 V/10 A output. Finally, the conclusion is given in Section VI.

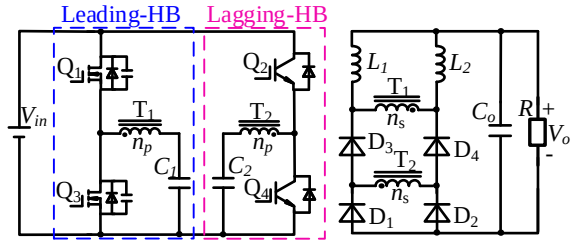

Fig.1 Proposed ZVZCS dual half-bridge converter.

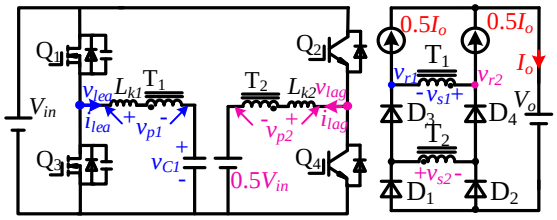

Fig.2 Simplified equivalent of the proposed converter.

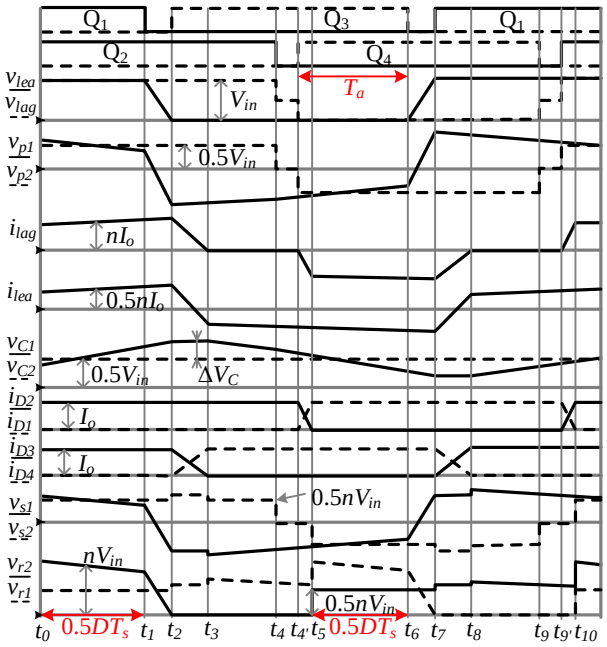

Fig.3 Key waveforms of the proposed converter.

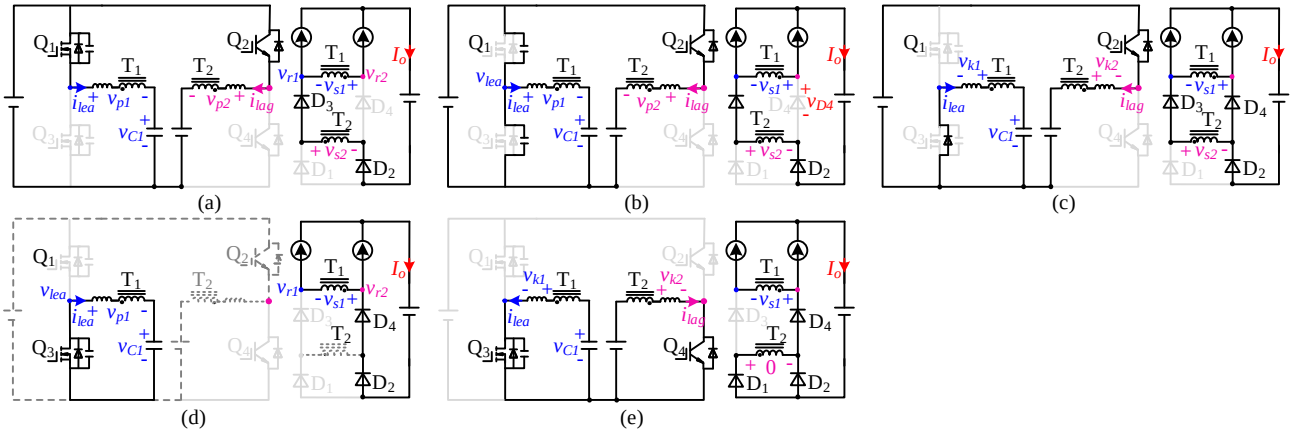

Fig.4 Equivalent circuits in the first half cycle. (a) *Mode 1* [t_0~t_1]; (b) *Mode 2* [t_1~t_2]; (c) *Mode 3* [t_2~t_3]; (d) *Mode 4* [t_3~t_4]; (e) *Mode 5* [t_4~t_5].

II. Operation Principle

Fig.2 shows the simplified equivalent circuit of the proposed converter. The leading-leg switches Q_1-Q_3 are MOSFETs with parasitic diodes and junction capacitors. The lagging-leg switches Q_2-Q_4 are IGBTs and only parasitic diodes are considered. The leakage inductors of transformers T_1 and T_2 are L_{k1} and L_{k2}, respectively. The turns ratios n_p:n_s of T_1 and T_2 are 1:n. The capacitances of C_2 and C_o are large enough to be treated as voltage sources of $0.5V_{in}$ and V_o, respectively. The voltage ripple of C_1 is ΔV_C. The output filter inductors L_1 and L_2 are large enough to be considered as constant current sources, and the values are equal to half of output current.

Fig.3 shows the key operational waveforms in steady state. T_a means the phase-shifted time between the driver signals of leading switches Q_1-Q_3 and lagging switches Q_2-Q_4, and its precise value is equal to the interval of [t_4'~t_6]. The output voltage is regulated by adjusting T_a. T_s is switching period of primary switches and D is duty-cycle of rectified voltage. D is equal to $T_a/0.5T_s$ if the durations of soft-switching transitions are ignored. As shown in Fig.3, each switching period compose of two half cycles (t_0-t_5 and t_5-t_{10}), which can be divided into ten switching modes. Since the operations are symmetric, only the first half cycle is introduced in this paper. Fig.4 shows the corresponding equivalent circuits.

Mode 1 [t_0~t_1]: In this mode, Q_1-Q_2 and D_2-D_3 are in on-state. The current $i_{lag}(t)$ and voltage v_{p2} of lagging-HB are nI_o and $0.5V_{in}$, respectively. The rectified voltage v_{r1} is equal to the secondary voltage of T_2 and it is $0.5nV_{in}$. The leading-leg current $i_{lea}(t)$ is $0.5nI_o$, which results in the linear increase of blocking capacitor C_1 voltage. This mode is called duty-cycle interval and the length of this mode is approximately $0.5DT_s$. The key voltages in this mode are given by

$$v_{C1}(t) = 0.5V_{in} - \Delta V_C + 0.5nI_o(t-t_0)/C_1 \quad (1)$$

$$v_{p1}(t) = V_{in} - v_{C1}(t) \quad (2)$$

$$v_{r2}(t) = nV_{in} + n\left[\Delta V_C - 0.5nI_o(t-t_0)/C_1\right] \quad (3)$$

Mode 2 [t_1~t_2]: *Mode 2* starts when Q_1 is turned off at t_1. In order to simplify the analysis, all currents are considered as constant and the voltage ripple of C_1 is neglected during this mode. The currents and voltages of lagging-HB are the same as in *Mode 1*. The key voltages can be calculated as follows:

$$v_{lea}(t) = V_{in} - 0.5nI_o(t-t_1)/2C_{oss} \quad (4)$$

$$v_{s1}(t) = n\left[v_{lea}(t) - 0.5V_{in}\right] \quad (5)$$

$$v_{s2}(t) = 0.5nV_{in} \quad (6)$$

The voltage across D_4 is

$$v_{D4}(t) = v_{s2}(t) + v_{s1}(t) = nv_{lea}(t) \quad (7)$$

Therefore, $v_{D4}(t)$ and $v_{lea}(t)$ decrease linearly, and they simultaneously fall to zero at t_2. Then, the body diode of Q_3 and D_4 start to conduct, and Q_3 can be turned on with ZVS. The length of this mode is $4V_{in}C_{oss}/nI_o$.

Mode 3 [t_2~t_3]: During this mode, the commutation between D_3 and D_4 is progressed and the secondary windings of T_1 and T_2 are paralleled. The voltage of C_1 is maintained at $0.5V_{in}+\Delta V_C$. The voltages across leakage inductors are expressed as follows:

$$v_{k1}(t) = \frac{L_{k1}}{L_{k2}+L_{k1}}\Delta V_C\,,\ v_{k2}(t) = \frac{L_{k2}}{L_{k2}+L_{k1}}\Delta V_C \quad (8)$$

The voltage across D_1 is calculated as

$$v_{D1}(t) = n(0.5V_{in} + v_{k2}(t)) = 0.5nV_{in} + \frac{nL_{k2}}{L_{k2}+L_{k1}}\Delta V_C \quad (9)$$

The leading current $i_{lea}(t)$ and lagging current $i_{lag}(t)$ decrease linearly because of the existence of $v_{k1}(t)$ and $v_{k2}(t)$. At the end of this mode, $i_{lag}(t)$ falls to zero, and the commutation between D_3 and D_4 finishes. The reverse voltage of D_3 is ΔV_C. Since ΔV_C is very small, D_3 can be considered to be turned off without reverse recovery loss.

Mode 4 [t_3~t_4]: During this mode, all the currents of lagging-HB are maintained at zero and only the leading-HB transfers the primary power to the secondary side. The leading current $i_{lea}(t)$ is maintained at $-0.5nI_o$ and the blocking capacitor C_1 is linearly discharged by $i_{lea}(t)$. This mode is defined as freewheeling interval since the rectified voltage $v_{r2}(t)$ is zero. The duration time of this mode is about $0.5(1-D)T_s$ if the soft-switching transitions are ignored. The key voltages are expressed as follows:

$$v_{C1}(t) = 0.5V_{in} + \Delta V_C - 0.5nI_o(t-t_3)/C_1 \quad (10)$$

$$v_{r1}(t) = nv_{C1}(t) \quad (11)$$

Mode 5 [t_4~t_5]: Since the lagging current remains at zero, Q_2 can be turned off with zero current at t_4. Then, Q_4 is turned on with zero current after a short dead-time. The commutation between D_1 and D_2 starts to progress, and the secondary voltage

of T_2 is clamped to zero. The voltage of C_2 appears on L_{k2}, and $i_{lag}(t)$ rise linearly in the negative direction. $i_{lag}(t)$ reaches to $-nI_o$ at t_5. At the same time, D_2 is turned off and the commutation between D_1 and D_2 finishes. This mode is the end of the first half cycle. The length is about $2nI_oL_{k2}/V_{in}$.

Mode 6-10 [t_5~t_{10}]: The second half cycle starts at t_5, and the operations during [t_5~t_{10}] are similar to the first half cycle.

III. Theoretical Analysis

A. Voltage gain

The output voltage is determined by duty-cycle D and its value is equal to the average of rectified voltage. Fig.5 shows the simplified waveforms of rectified voltages and currents flowing through inductors in the traditional converter and in the traditional proposed converter.

For the traditional converter, the voltage gain is given by

$$G_{tra}(D) = V_o / nV_{in} = 0.5D \tag{12}$$

The voltage gain for the proposed converter is calculated as

$$G_{pro}(D) = V_o / nV_{in} = 0.5D + 0.25 \tag{13}$$

As shown in Fig.5, the rectified voltages in the proposed converter and in the traditional converter are three-level and two-level waveforms, respectively. The primary energy transmission is continuous in the proposed converter while it is discontinuous in the traditional converter. Therefore, $G_{pro}(D)$ is greater than $G_{tra}(D)$. The converter with higher voltage gain can obtain lower voltage stress of rectified diodes and turns ratio of transformers, which will contribute to the improvement of efficiency.

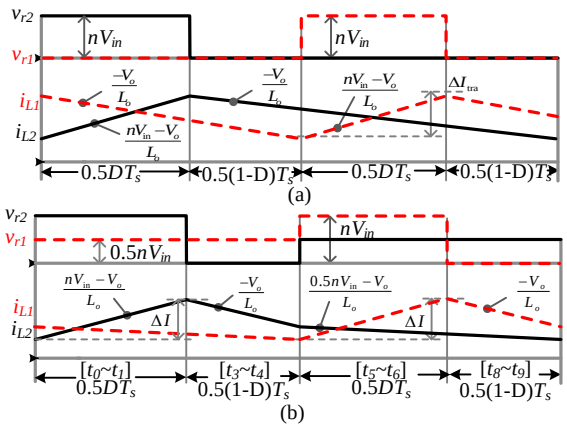

Fig.5 Simplified waveforms of voltages and currents (a)in the traditional converter, (b) in the proposed converter.

B. Current ripple of output filter inductors

The output filter inductor is considered as a constant current source and its current ripple is ignored when the operation principle is introduced in Section II. This part focuses on the theory analysis about current ripple of output filter inductor. In order to simplify analysis, only the intervals of [t_0~t_1], [t_3~t_4] and [t_5~t_6], [t_8~t_9] are considered. In fact, the voltage ripple ΔV_C of C_1 is small, so its effect on the current ripple is ignored. The current ripple is mainly decided by the rectified voltage and it can be calculated based on Fig.5

For the proposed converter, the current ripple is calculated as

$$\Delta I_{pro} = \frac{0.5T_sV_o}{L_o}\frac{D(1.5-D)}{D+0.5} \tag{14}$$

where L_o is the value of output filter inductor.

For the traditional PSFB converter with CDR, the current ripple is

$$\Delta I_{tra} = \frac{0.5T_sV_o}{L_o}(2-D) \tag{15}$$

The current ripple ratio of the proposed converter to the traditional converter is described as

$$k(D) = \frac{\Delta I_{pro}}{\Delta I_{tra}} = \frac{D(1.5-D)}{(D+0.5)(2-D)} \tag{16}$$

In the traditional converter, the rectified voltages are zero during the interval of $0.5(1\text{-}D)T_s$, as shown in Fig.5(a). The primary power cannot be transferred to the output side and the constant output power is realized by using the energy stored in the output filter, which will significantly increase the filter requirement. On the other hand, the rectified voltages in the proposed converter are not zero simultaneously during the whole switching period, as shown in Fig.5(b). The primary power can be continually transferred to the output side. Fig.6 shows the plot of ratio $k(D)$ versus duty-cycle D. The current ripple in the proposed converter is much lower than that in the traditional converter. Lower current ripple is beneficial for the reduction of current stress and power loss.

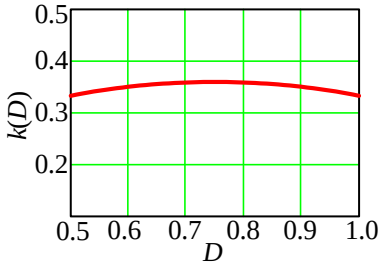

Fig.6 Ratio $k(D)$ versus duty-cycle.

C. Voltage ripple of block capacitor C_1

In order to simplify the calculation of voltage ripple, the ZVS transition intervals are ignored. As shown in Fig.3, both the charging current and discharging current of C_1 are $0.5nI_o$, and the durations are about $0.5T_s$. Therefore, the voltage ripple of C_1 can be calculated as follows:

$$\Delta V_C = nI_oT/8C_1 \tag{17}$$

D. ZVS condition for the leading switches

The ZVS operation of leading switches is achieved during *Mode 2*, and it is less sensitive to load current since the output filter inductors take part in the ZVS transition, like that of leading switches in the traditional PSFB converter. The ZVS transition time is given by

$$T_{12} = 4V_{in}C_{oss}/nI_o \tag{18}$$

Therefore, the ZVS condition for the leading switches in the proposed converter is not usually required in terms of the required ZVS energy. In order to ensure the junction capacitors discharged completely, the dead-time between leading switches should be larger than T_{12}.

E. ZCS condition for the lagging switches

During *Mode 3*, the lagging current is reset by the voltage ripple of C_1. The resetting time is given by

$$t_{ZCS} = nI_o(L_{k1}+L_{k2})/\Delta V_C \tag{19}$$

In order to ensure that the lagging current has enough time to decay to zero, t_{ZCS} should be smaller than $0.5(1\text{-}D)T_s$. Therefore, the ZCS condition of lagging switches is given by

$$D_{\max} \le 1-2nI_{o\max}(L_{k1}+L_{k2})/\Delta V_C T_s \tag{20}$$

where $D_{\max}$ means the maximum duty-cycle and $I_{o\max}$ means the maximum load current.

F. Primary circulating current

Fig.7 shows the key primary voltages and currents of main transformers in the traditional PSFB converter and in the proposed converter. As shown in Fig.7(a), the primary voltage v_p is zero although the primary current i_p is maintained constant during the interval of $0.5(1\text{-}D)T_s$. Thus, the energy transmission is zero and there is primary circulating current in the traditional converter, which will increase the conduction loss and output filter requirement. On the other hand, in the proposed converter, the voltage and current of leading-HB transformer always have positive or negative values during the whole switching period, and the current of lagging-HB transformer falls to zero during the interval of $0.5(1\text{-}D)T_s$, as shown in Fig.7(b). Therefore, the primary energy can be continually transferred to the secondary side through the leading-HB transformer and the circulating current is removed in the proposed converter.

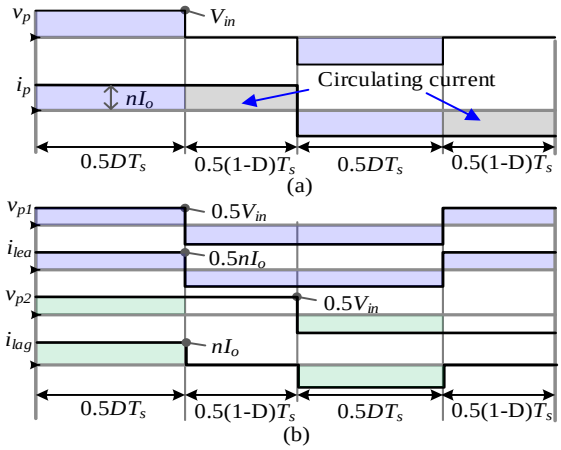

Fig.7 Simplified waveforms of primary voltages and currents (a) in the traditional converter and (b) in the proposed converter.

IV. Design Considerations

For the purpose of performance comparison, two 1-kW experimental prototypes based on the proposed converter and the traditional CDR converter are designed, respectively. The prototypes are designed with the following parameters:

Input voltage: V_{in} = 300~380 V;
Output voltage: V_o = 100 V;
Maximum output current: I_{omax} = 10 A;
Switching frequency: f_s = 60 kHz.

A. Turns ratio of main transformers

The turns ratio is mainly determined by the relationship between input voltage and output voltage and it should be designed to guarantee that the output voltage is constant under the lowest input voltage condition. Based on (13), the turns ratio in the proposed converter is calculated as

$$n=\frac{2V_o}{(0.5+D_{\max})V_{in}} \tag{21}$$

Considering the resetting and transition time, the maximum duty-cycle $D_{\max}$ is preset 0.80 at the lowest input voltage, *i.e.* 300 V, then n = 0.52. Since the total power is shared by two transformers, small-sized magnetic cores can be used. In this paper, the transformers are made to use two PQ3535 cores, and their turns are designed as n_p:n_s = 27:15. The measured leakage inductances are L_{k1}= L_{k2}=5 μH.

In the traditional converter, a large-sized magnetic core is required since the primary energy is transferred to the secondary side only through one transformer. The transformer is made to use one PQ5050 core. The turns ratio n_{tra} is calculated based on (12) and the value is 0.84.

Table I shows the parameters of used magnetic cores. As shown in Table I, the total volume, weigh and core loss of two PQ3535 cores are smaller than those of PQ5050 core. Therefore, the use of two small-sized transformers instead of a large-sized transformer contributes to the improvement of power density, conversion efficiency and overall performance.

TABLE I
PARAMETERS OF USED MAGNETIC CORES [35,36]

Core	Volume (mm^3)	Weigh (g)	Loss (W)*
2*PQ3535	2*16300	2*73	2*10
PQ5050	37100	195	23

*Test conditions: 100 kHz, 200 mT, 100 ℃

B. Selections of semiconductors

In the full-bridge converter, the voltage stress of primary switch is clamped at input voltage by the body diode. According to the operational waveforms in Fig.3, the current stresses of leading switches Q_1-Q_3 and lagging switches Q_2-Q_4 are $0.5nI_o$ and nI_o, respectively. For the proposed converter, Q_1-Q_3 and Q_2-Q_4 are selected as FQP12N60 (MOSFET, 600 V, 10.5 A) and STGP5H60 (IGBT, 600 V, 10 A), respectively. For the traditional converter, all the primary switches are selected as FQP12N60.

If the oscillation of rectified voltage caused by the leakage inductors and parasitic capacitors of diodes is ignored, the voltage stresses of D_1-D_2 and D_3-D_4 are $0.5nV_{in}$ and $nV_{in}+n\Delta V_C$, respectively. The voltage stress of D_1 and D_2 is much lower than that of D_3 and D_4. In this paper, D_1-D_2 are selected as schottky diode 12TQ150 (150 V, 15 A) and D_3-D_4 are selected as STTH20L03 (300 V, 20 A). The voltage stress of rectified diodes in the traditional converter is $n_{tra}V_{in}$ and it is much larger than that in the proposed converter. The rectified diodes in the traditional converter are selected as STTH15L06 (600 V, 15 A).

C. Blocking capacitors

The voltage ripple of blocking capacitor C_1 has a significant effect on the performance of proposed converter. According to (20), ΔV_C should be as large as possible to reduce the resetting time and to extend the ZCS range of lagging-leg switches. Conversely, ΔV_C should be minimized to weaken the effect on voltage gain and voltage stress of rectified diodes. Therefore, a tradeoff should be made in the design process. In general, the

voltage ripple is set around 10% of V_{in} under the maximum output current. Then, the value of C_1 can be calculated according to (17). On the other hand, C_2 is regarded as a constant voltage source in the above analysis and its value should be as large as possible. In this paper, C_1 and C_2 are selected as 250 nF and 2 μF, respectively.

D. Verifications of ZVS and ZCS conditions

In order to guarantee that the junction capacitors are completely discharged during *Mode 2*, the dead-time of leading –leg should be longer than the discharging time. From this point of view, the worst case is the minimum load current. The ZVS range of the experimental prototype is 10% to full load. According to (18), the discharging time of leading-leg is about tens of nanosecond. The dead-time of leading-leg is set as 120 ns considering the design margin for the real implementation.

The maximum resetting time of lagging-leg current is determined from (19) and its value is about 1.2 μs. The maximum duty-cycle is preset 0.80 in this paper and the allowable resetting time is 1.7 μs. Therefore, the ZCS condition is easily satisfied and the lagging-leg switches can realize ZCS operation over the whole line and load ranges.

E. Detailed comparison with the existing DT-FB converters

The DT-FB converters with FBR [27] and CTR [26] are selected to be compared with the proposed converter in this section. Table II summarizes the characteristics of these three DT-FB converters.

For the FBR and CTR converters, both the ideal voltage gains are 0.5(D+1), and their ratios of maximum value (D = 1) to minimum value (D = 0) are 2. For the proposed CDR converter, the voltage gain is 0.5(D+0.5), and the ratio is 3. Therefore, the CDR converter can achieve a wider input or output voltage range compared to the others. It should be noted that the voltage gain of proposed converter is smaller than that of other converters, which results in the increase of voltage stress of diodes and turns ratio of main transformer.

The maximum voltage stress of diodes in FBR, CDR and CTR are nV_{in}, $nV_{in}+n\Delta V_C$, and $2nV_{in}$, respectively. Therefore, FBR/CTR withstands the lowest/highest voltage stress, and it suits for high/low output voltage applications. The voltage stress of diodes in CDR is in the middle of FBR and CTR, thus, the proposed CDR converter suits for the application with medium output voltage.

The current stress of leading switches in CDR is about $0.5nI_o$ while they are nI_o in FBR and CTR. Therefore, the conduction loss of leading switches in CDR is considerably reduced since it is proportional to the square of current. These three converters have nearly the same current stress of lagging switches. But the CDR converter can still achieve lower conduction loss because IGBTs are employed and they have lower conduction loss compared to MOSFETs.

As shown in Table II, the total number of rectified diodes and secondary side windings in FBR, CTR and CDR are 8,8, and 6, respectively. Therefore, the structure of proposed converter is the simplest among these three converters.

All the primary switches in the FBR and CTR converters are operated with ZVS. The ZVS is achieved by using the energy stored in the inductive devices E_{ind} to discharge the junction capacitors. The ZVS condition is that E_{ind} should be larger than the stored energy of junction capacitors E_{cap}. E_{ind} depends on the output current and it can be enlarged by increasing the magnetizing current ΔI_m, which will result in high turn-off loss and magnetic core loss. This is contrast to the fact that in the proposed converter, the soft-switching condition is independent on the operational condition and it is easy to satisfy by presetting suitable dead-time and maximum duty-cycle, as described in the previous section.

TABLE II
CHARACTERISTICS OF THE DT-FB CONVERTERS WITH FBR, CTR AND CDR

Topology	FBR	CTR	CDR
Voltage gain	0.5(D+1)	0.5(D+1)	0.5(D+0.5)
Maximum voltage stress of diodes	nV_{in}	$2nV_{in}$	$nV_{in}+n\Delta V_C$
Current stress of leading switches	nI_o	nI_o	$0.5nI_o$
Current stress of lagging switches	$nI_o+\Delta I_m$	$nI_o+\Delta I_m$	nI_o
Number of diodes and secondary side windings	6+2	4+4	4+2
Soft-switching condition	$E_{ind} > E_{cap}$	$E_{ind} > E_{cap}$	Equations (17) and (19)

F. Loss analysis

The power loss distributions of the proposed converter and the traditional converter are analyzed and compared in this section. In order to simplify the theoretical analysis, only the losses of semiconductor and magnetic components are considered since they are the main contributor to the total power loss. Fig.8 shows the calculated loss distributions at different load currents. As shown in Fig.8, due to low collector-emitter saturation voltage of IGBT and current ripple of filter inductors, the losses of primary switches and inductors in the proposed converter are lower than those in the traditional converter over the entire load range, which is the most outstanding characteristic of the proposed converter. Moreover, the losses of rectifier and transformers in the proposed converter are also lower at light loads. At heavy loads, the conduction loss makes up most of the total power loss, but the forward voltage drop of rectified diodes and winding resistance of transformer in the proposed converter are higher than those in the traditional converter, which will limit the further improvement in efficiency.

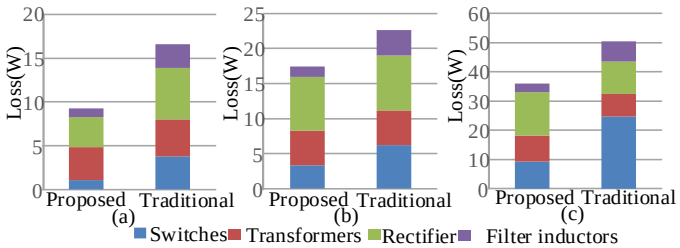

Fig.8 Loss distributions at V_{in} =380 V, (a) 20% of full load (b) 50% of full load (c) 100% of full load.

V. Experimental Results

An experimental prototype based on the proposed converter is built to verify the theory analysis, as shown in Fig.9. In addition, a prototype based on the traditional CDR converter is also built for the purpose of performance comparison. The main components are selected according to Section IV.

The length of each mode is measured through the experimental prototype. Table III shows the measured results at I_o = 10 A and V_{in} = 380 V. As shown in Table III, the lengths of *Mode 2*, *Mode 3* and *Mode 5* are negligible compared with that of *Mode 1* and *Mode 4*. Fig.10 shows the primary experimental waveforms in the proposed converter. It can be noted from Fig.10(a) that both the current and voltage of leading-HB are non-zero during the whole switching period. Thus, the primary power can be continually transferred to the secondary side through the leading-HB and there is no circulating current in the leading-HB. On the other hand, the current of lagging-HB falls to zero during *Mode 3* and it is maintained at zero during *Mode 4*, as shown in Fig.10(b). This feature makes it possible to remove the primary circulating current and to achieve ZCS operation. The primary voltage of transformer T_1 is not square wave because of the voltage ripple of blocking capacitor C_1. The experimental results coincide well with the theory analysis.

TABLE III
Length of Each Mode

Mode	1	2	3	4	5
Length	3.8 us	0.06 us	1.06 us	3.27 us	0.14 us
Percentage	45.62%	0.01%	12.73%	39.26%	1.68%

Fig.11 shows the experimental waveforms of voltages across rectified diodes at I_o = 10 A and V_{in} = 380 V. It can be noted that the voltage stress of D_1 and D_2 is much lower than that of D_3 and D_4. Therefore, D_1 and D_2 are selected as schottky diodes 12TQ150 to reduce the conduction loss. Based on equation (9), the waveforms of v_{D1} and v_{D2} exist some small platforms during *Mode 3* and *Mode 8*, as shown in Fig.11. The platforms are used to force the commutation between D_1 and D_2. Moreover, the reverse voltages of D_3 and D_4 are very small, thus the turn-off losses can be ignored.

Fig.12 shows the experimental waveforms of rectified voltages and currents flowing through output filter inductors at different input voltages. As shown in Fig.12, the rectified voltages of the proposed converter are three-level waveforms. This feature contributes to the reduction of voltage stress of rectified diodes and current ripple of inductors.

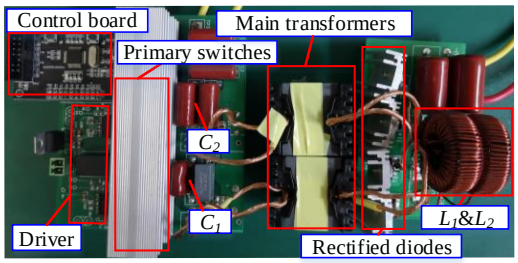

Fig.9 Photograph of the proposed converter.

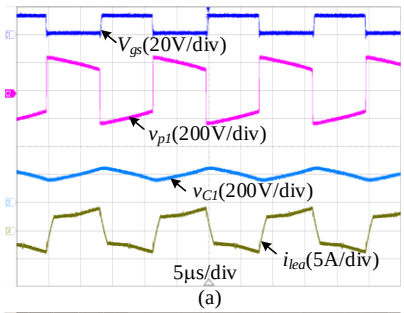

Fig.10 Primary waveforms in the proposed converter: (a) leading-HB, (b) lagging-HB.

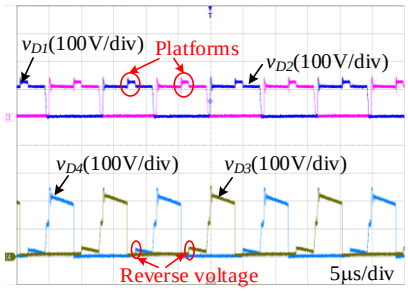

Fig.11 Experimental waveforms of voltages across rectified diodes.

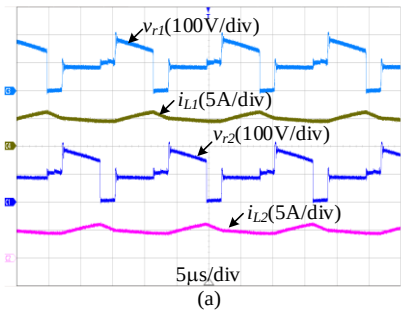

Fig.12 Key secondary waveforms at different input voltages: (a) V_{in} = 300 V; (b) V_{in} = 380 V.

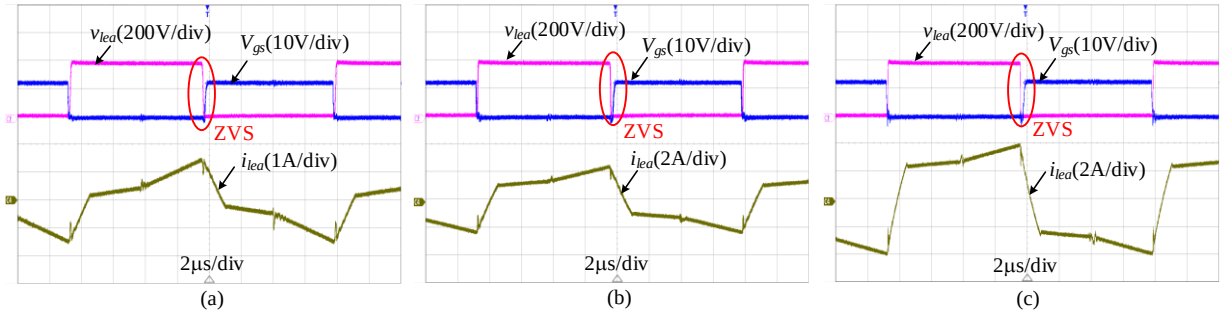

Fig.13 ZVS waveforms of leading switches at different load currents: (a) 2 A; (b) 5 A; (c) 10 A.

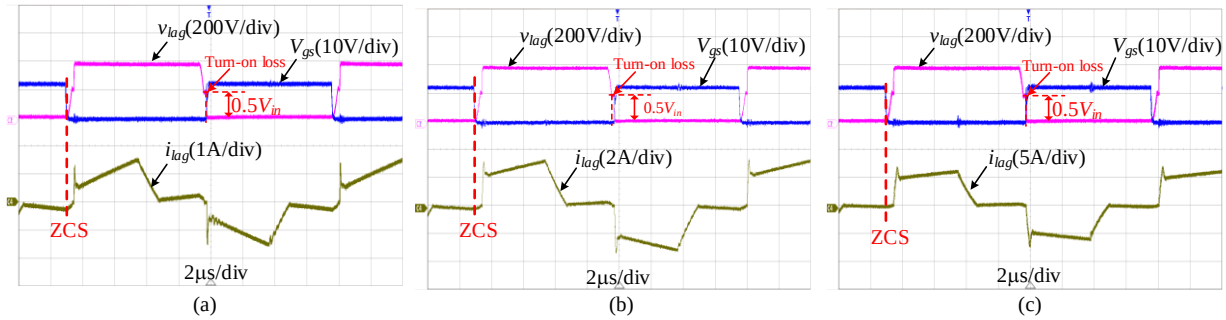

Fig.14 ZCS waveforms of lagging switches at different load currents: (a) 2 A; (b) 5 A; (c) 10 A.

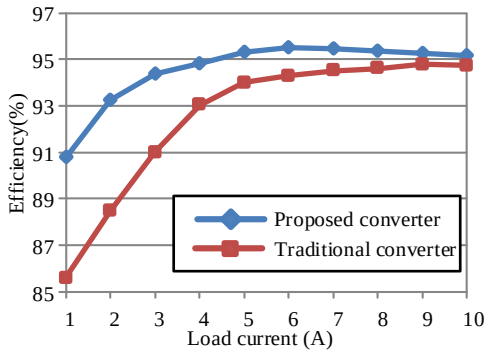

Fig.15 Experimental efficiency at V_{in} = 380 V.

Fig.13 shows the experimental ZVS waveforms of leading switches at different load currents. As shown in Fig.13, the drain-to-source voltage across the leading switch attains zero before the gating signal is applied. The experimental results confirm ZVS turn-on of leading switches. It should be noted that there are three rising slopes in the experimental waveform of i_{lea} which is not consistent with the theory analysis in Fig.3. This is because the current ripples of output filter inductors are ignored in Section II.

Fig.14 shows the experimental ZCS waveforms of lagging switches. It can be noted from Fig.14 that the lagging current i_{lag} is zero when the switch is turned off, which indicates that the lagging switches operate with ZCS. As shown in Fig.14, the lagging voltage v_{lag} starts to decrease after one of the lagging switches is turned off and it is maintained $0.5V_{in}$ during the dead-time of lagging-HB. This is due to the fact that the magnetizing current of T_2 can be used to discharge the junction capacitors of IGBTs. The lagging switches are turned on with $0.5V_{in}$, which results in turn-on loss. In fact, the turn-on loss of IGBT can be ignored since the junction capacitor of IGBT is very small.

Fig.15 shows the experimental efficiency comparison between the traditional PSFB converter with CDR and the proposed converter at V_{in} = 380 V. As shown in this figure, the proposed converter obtains higher conversion efficiency than the traditional converter in the entire measured power range since it has a wide soft-switching range, improved rectified voltages and low conduction loss.

VI. Conclusion

This paper proposes a ZVZCS DT-FB converter with CDR. Two separate transformers and output filter inductors are employed in the proposed converter. By adopting such structure, the leading-leg and lagging-leg switches can achieve ZVS and ZCS operations over a wide load range, respectively. The primary circulating current is removed. Moreover, the proposed converter can obtain three-level rectified voltages and the primary energy is continually delivered to the secondary side during the whole switching period. Due to these features, it is possible for the proposed converter to achieve better performance and higher conversion efficiency compared with the traditional PSFB converter with CDR. A prototype based on the proposed converter is designed and tested to verify the theoretical analysis. Experimental results show that the proposed converter is a promising solution to the applications with high power and variable input voltage.

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